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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,903	02/28/2002	Andy Wei	AMD1:115/HON	4163
7590 03/04/2004			EXAMINER	
Timothy M. Honeycutt, Attorney at Law P.O. Box 1577 Cypress, TX 77410-1577			LEE, HSIEN MING	
			ART UNIT	PAPER NUMBER
			2823	
DATE MAILED: 03/04/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/085,903

Applicant(s)

WEI ET AL.

Examiner

Hsien-Ming Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 6-17 and 20-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4, 6, 14-17, 20 and 28-33 is/are allowed.
- 6) ☒ Claim(s) 21 and 25-27 is/are rejected.
- 7) ☒ Claim(s) 7-13 and 22-24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Remarks*

1. The final rejection is withdrawn.
2. The objection to claim 7, as set forth in the previous Office action, has not been responded by applicants.
3. Claims 1-4, 6-17 and 20-33 are pending in the application.

### *Claim Objections*

4. Amended claim 7 is objected to because of the following informalities: lacking antecedent basis, i.e. "the semiconductor-on-insulator substrate." Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 21 and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimi et al. (US 5,698,869).

In re claims 21 and 25, Yoshimi et al. disclose a circuit device, wherein the device comprises a gate electrode 205, comprising:

- a semiconductor-on-insulator substrate 201/202/Si layer having a device region 203/206/207;

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- an impurity region 206/207 in the device region 203/206/207, the impurity region 206/207 defining a **singular** junction 215 (col. 4, lines 30-33); and
- a first dislocation region D (i.e. a region comprising a plurality of dislocations located at left side of 203) and a second dislocation D ( i.e. a region comprising a plurality of dislocations located at right side of 203) in the device region 203/206/207, the first and second dislocation regions D being in **non-parallel** (i.e. the first dislocation region on the left side of 203 are pointing to **left upper corner**, whereas the second dislocation region on the right side of 203 are pointing to **right upper corner**) spatial relationship and traversing the singular junction 215 (col. 4, lines 30-33, where it states “ .... .. to traverse the pn junction interface **215** over the drain region **206** and the channel region **203**.”)

In re claim 26, Yoshimi et al. also teach comprising a plurality of dislocation regions (i.e. the aforementioned first and second dislocation regions) traversing the pn junction 215.

In re claim 27, Yoshimi et al. also teach that the device region 203/206/207 comprises silicon because the device region comprises Si and Ge (col. 4, lines 15-30 and col. 2, lines 39-53).

***Allowable Subject Matter***

7. Claims 1-4, 6, 14-17, 20 and 28-33 are allowed.
8. Claims 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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9. Claims 8-13 are objected to as being dependent upon an objected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

Yoshimi et al. to US 5,698,869 neither teach nor suggest forming a *buried* amorphous region in the device region; forming a source/drain *extension* region and *another* impurity region *overlapping* the source/drain extension region; and the first dislocation region traversing the *first junction* and the second dislocation region traversing the *second junction*.

#### ***Response to Arguments***

11. Applicant's arguments filed 10/9/03 have been fully considered but they are not persuasive.

In re claim 21, applicants argued that “[t]he features identified in Yoshimi et al. as crystal defects in FIG. 7 are parallel in space.” (fifth paragraph, page 9)

Contrary to the argument, Fig. 7 clearly illustrates that the first dislocation region D, which is equivalent to the one on the left side of 203, are pointing to **left upper corner**, whereas the second dislocation region D, which is equivalent to the one on the right side of 203, are pointing to **right upper corner**. Obviously, the aforementioned two dislocation regions are **not parallel** in space. The two dislocation regions D would traverse the **singular** pn junction 215. Particularly, Yoshimi et al clearly indicate that the crystal defects D traverse the pn junction **interface 215** (col. 4, lines 30-33 and col. 34, lines 58-61), **not plural interfaces**.

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12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee  
Examiner  
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Feb. 24, 2004